Common Heterogeneous Integration and Intellectual Property (IP) Reuse Strategies (CHIPS)

Daniel S. Green

U.S. Defense Advanced Research Projects Agency (DARPA)

CHIPS Proposers Day Falls Church, VA

September 21, 2016





<u>Purpose of this meeting</u>:

- Discuss program objectives and structure.
- Provide opportunity for teaming prior to proposal deadline

Program not final until BAA published

Please consult published BAA for final program specifics

Once BAA published and until the deadline for receipt of proposals

- Open communications between proposers and the program manager are encouraged.
- But: Information given to one proposer must be available to all proposers.
- The best way to get a question answered is to email it, and to retrieve your answer from the Questions and Answers list via the MTO solicitations website.
- Note that any question that contains distribution restrictions, such as 'company proprietary', will not be answered.

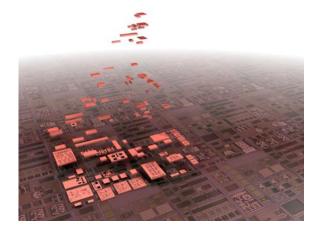
Questions:

DARPA-BAA-16-62@darpa.mil

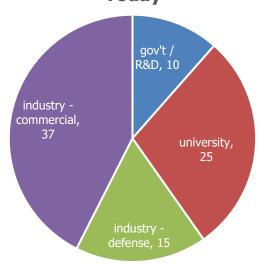


DARPA Welcome to the CHIPS Proposers Day

- 08:00-09:00: Registration
- 09:00-09:15: Bill Chappell Opening Remarks
- 09:15-10:15: Dan Green CHIPS Overview
- 10:15-10:30: Break
- 10:30-12:00: Presentations
 - 10:30-10:45: AMD Bryan Black
 - 10:45-11:00: Adapteva Andreas Olofsson
 - 11:00-11:15: GlobalFoundries Ajit Dubey
 - 11:15-11:30: X-Celeprint Chris Bower
 - 11:30-11:45: Northrop Grumman Augusto Gutierrez-Aitken
 - 11:45-12:00: Summary Dan Green
- 12:00-13:30: Lunch (self-organized)
- 13:30-15:30: Poster session and networking
- 15:30-16:00: Working with DARPA Dan Green
- 16:00-16:30: BAA Q&A Dan Green
- 16:30-17:00: Concluding Remarks Dan Green



Organizations Participating Today

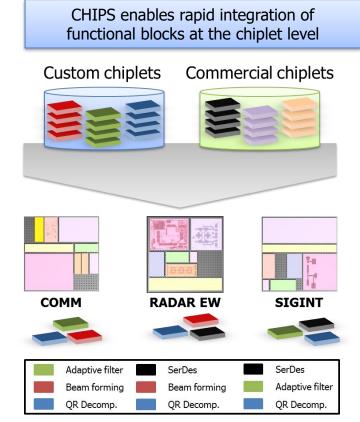




CHIPS will develop **design tools, integration standards, and IP blocks** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.



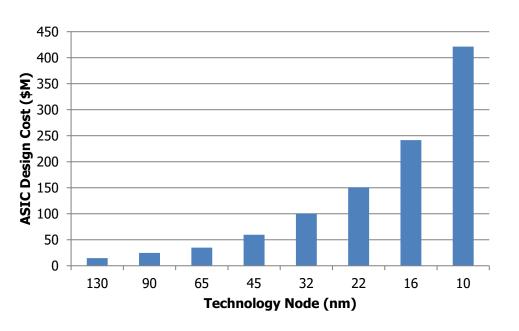






Why CHIPS? Advanced Si is Expensive...

Expensive to design at advanced nodes ...



... which some commercial products can support ...



© apple.com

Fab cost for commercial electronics amortized over **one day's** worth of iPhones

... but DoD cannot.

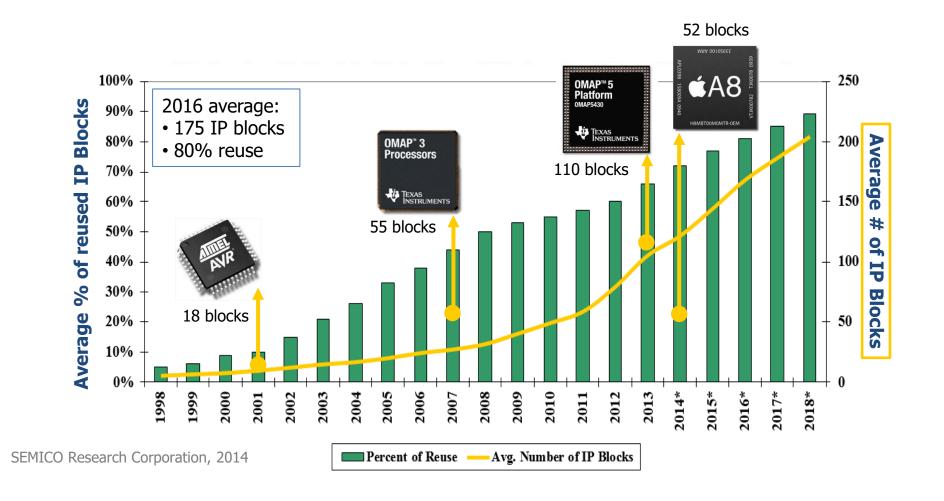


Fab cost for a DoD IC amortized over **entire 29-year** acquisition of JSF

Source: "Cashing in with Chips" AlixPartners Semiconductor R&D outlook report, 2014.



...and IP Reuse is Common for Multicore SoCs...

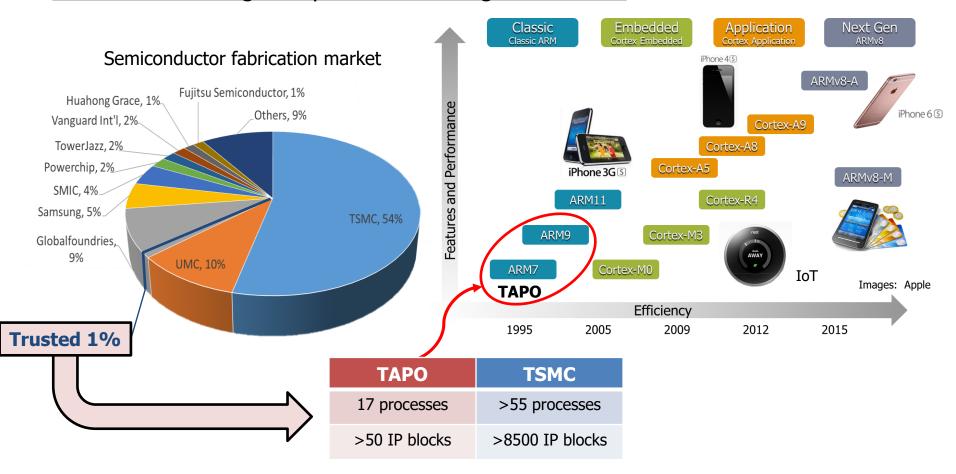


IP Reuse is increasingly important and shows no signs of slowing



DARPA ...but Challenging for the DoD

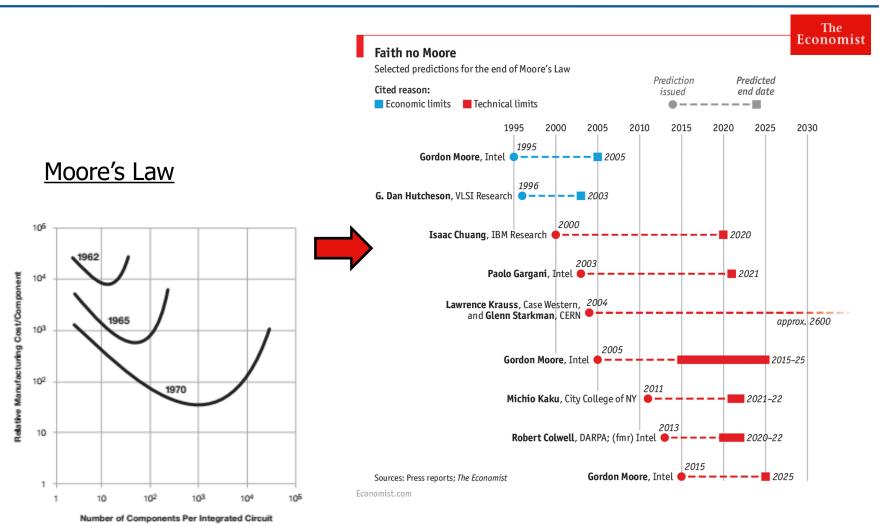
<u>Limited access to global pool of knowledge **and** talent</u>



CHIPS is designed to expand the pool of IP and design resources



End of Moore's Law?



End of Moore's Law means everyone is becoming low volume



DARPA Moore's Law INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.

The experts look ahead

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director Passarch and Econograph Laboratories, Paintible Santimordanter

The future of integrated electronists is the firmer of electronus itself. The advantages of integration will bring about a - widdow, the improved reliability much possible profiferation of electronics, pushing this selence into many

lesqueed circuits will lead to save worders as here: compaten-oral least remainals swince and as a seniral compage-automatic controls for automobiles, and present portable communication equipment. The electronic wrinwas through early a display to be familia today.

that the biggest potential lies in the production of large eras. In telephone communications, imaginary circuits to digital filters will separate change to on matriples againmere. Emegrated circuits will also switch wisphone circuits and perform data processing.

Computers will be need personful, and will be organized in completely different ways. For example, numerics had t of integrated electronics may be distributed throughout the

The extract III was in the set of the extract III was not to the principal schemes where there is necessarily to the extract of the extract III was set of the extract III was set of the extract III was set of the extract III was not at III to despise in pulsarility in the extract III was not the fulfill the extract III was not the

Markings should be to those in existence traffin lower costs and with lister term-around.

Present and future

By integrated dimaliacies which are reflered to as microelectr vell to any additional ones that result in cits tions napplied to the user as irriduable units lest was to a foliage les electronics e galaxie at municipy complex electronic functions in line minimum weight. Several approaches evelstemanumbly techniques for incly that con (Tim structures and semiconductor integrated a

Each approach evolved rapidly and const such borrowed aphalques from another. Many believe the way of the fature to be a combined

The advocator of numbers ductor integra a builty using the improved characteristics of t tion by applying each films directly to acception to substrate. These administring a technolog films are developing asphalicated techniques meet of active amazondant or devices to the p

in equipment takes

Electronics, Volume 35, Humber B. April 19, 1965



G. E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been Director of the research and development laboratories since 1959

Integrated electronics is a stablished today. By technique alread mandatury for renormalitary systems, nince the rehalf fee, six and weight required by some of them is adviceable only with integration. Such programs as Aprille, for manual reconflight, have demonstrated the reliability of laregrated electronics by showing that complete classic fina-tions are at fine from failure as the best individual crando-

machines in design or in early production employing imagined electrosics. These machines cost less and perform batter than those which use "conventional" electronics. instruments of various sorts, especially the repicity in-

practing numbers corplicating digital tachniques, are starting

The use of linear integrated circuity is still restricted. primarily to the military. Such imagrated functions are no persive and not available in the variety required to satisfy a major fraction of linear electronics. But the first applications are beginning to appear in constructed electronics, par-ficularly in equipment, which reads love-dequescy amplifyen of small stop

In almost every case, triagrated a lectronics has denote arrated high reliability. Does at the present level of production - law compared to that of discrete components - it offor reduced systems out, and in many systems improved performance has been realized.

Integrated electronics will make electronic techniques more generally available throughout all of society, perform ing more functions that present is are done madequartly by other techniques or not done as it. The principal advantages will be lower units and greatly simplified design—payoffs from a mady rapply of low-cost functional packages.

Formor applications, sentimed actor integrated circuits. will predominate. Seniconductor devices are the only reaconstitu candidates presently in anidotos for the active ele-ments of integrated circum. Puerro sentioordiscon elements look attraction too, because of their potential for low-cost and high reflechility, but they can be used only if propiation is not a price tequiate.

Silicon is likely to remain the busic material, although

others will be of me in specific applications. For example, pillium assentide will be important in integrated encoverer Emotions. But sillion will predominate it lower framewire because of the reshamings which has aboutly evolved around it and its made, and because it is an abundant and relatively inorporal to starting motorial.

Reduced cost is one of the big structures of integrated electronics, and the out advantage continues to increase or the trained agy evolves toward the production of larger and Constitues on a single service abother substrate For simple a soults, the cost per component is usually invested,

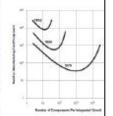
capitation place of sensionals are in the equivalent and up containing more components. But as components are added decreased yields more than compensate for the in complexity, tending to mise the cost per comp derring mindown our stary given trace in the e-

the imbaskep. At present it is reached when I nexts are used per circuit. But the restinue is rewhitethe entreous corners litting one prighter test sheed five years, a plot of costs suggests that name and yet compound raight be exceeded in a about 1,000 components per cincul (providing to functions on be enclased in contents must like. the manufacturing cost per component can be o

only a tooth of the prepart cost.

The complexity for minimum compressed commed at a case of rangitaly a Gatter of two pergraph on soit page). Curtainly over the shortte can be expected to pretines, if set to increase former party, the tape of increase in a bit more tax though there is no issues to believe it will not run constant for at least 18 years. This recently 1975 her of components per magnitud circuit for mine

With the dissessional telescopes already being degreed discrits, is sleed high pertin can be built on content two them and the of an inch of



There is no functionestal obstacle to active ing dening yields of 100%. All present, packaging costs or for exceed the cost of the anniouslant or drustee shelf that there is no security to improve yields, but they can be extend as high as

from soing the yield.

a two-milespace care also contain several hildrens of review is economically least to

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the components can be already packed with no space winted

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techniques and does not require the more exact techniques, and a celestron beam operations, which are being studied to

tance or a few clodes. This allows at have 500 components. the thermochanging equal printing moderations that other first per Brass lock or a quarter million per square lock. Thus, specify to electron recovers, it is not even recovery to do \$3.000 components need course only about one Conth is new Employee'd research or to replace present processes. Daily the organizating of art is accolled.
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of thousands of companying in a single alliant chip. If we could strink the refluence of a standard high-speed drail computer to that required for the components themdigital company to that alves, received dispect to glow bright hough present perver dissipation. But it was 1 happen with integrated circuits. Since integrated electric in tractures are two-dimensional, theybove a surfaceword bite for cooling close to each conterof Vest percention. It was fitten, power is needed printerly to sources. As long as a function is conflicted to a small argo as suissance which main by driven it distinctly finding. In fact, stricking chromotons on an intepossible to operate the separate at higher speed for the same power per unit ansa-

Day of reckening Clouds, we will it drie to build such component crammed equipment. Note, we selected what circumstances we should do it. The total control making aparticular system function must be minim out. To do so, we could amortise contof making aparticular system

the engineering over on and identical items, or enable fina-This techniques for the a ginearing of large functions so that no disproportionate explane need to home by a particular artis. Parkapunowly devised design automotion procedures without any operior organization.

It may prove to be more economical to belief large



Moore's Law INCLUDES Heterogeneous Integration

It may prove to be more economical to build large systems out of smaller functions, which are <u>separately pack</u>aged and interconnected. The availability of large functions.

combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly The experts look ahead and economically. Cramming more components onto integrated circuits contrator piece of sentronductor to the equivalent rankage Imported distroyles is established today. Intechnique. containing more components. But as components are abled alread mandatury for renoralitary systems, since the redecreased yields more than compensate for the in hald fee, six and weight required by some of them is adviseable only with integration. Such programs as Aprille, for complexity, tending to mise the cost per comp theretis a mindrates containing given time in the e manuel races flight, have demonstrated the reliability of inthe imbra-logs. At present, it is reached when With unit cost falling as the number of components per natural electronics by showing that complete circuit finecircuit rises, by 1975 economics may dictate eque many as 65,000 components on a single silicon of By Gordon E. Moore Director: Pleasanth and Development Laboratories, Paintible Bands The future of integrated electronists is the firmer of electron-More is itself. The advantages of integration will bring should **W350**+ profiferation of electrowics, profring this selected into many Integrated circuits will lead to savit worders as hene. No barrier exists comparable to compared on a local tension because of a committed conthe thermic has an in equal whom a molderation, that other field page-automatic controls for automobiles, and presinal portable communication equipment. The electronic wrinmy familiarental research or to replace present processeswarshrivede only a display to be familifu today. Only He organizates of at a world.

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It may prove to be more economical to belief lary degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He



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Conventional Assembly Has Attractive Features for HI ... But Isn't Keeping Up on Pitch and Performance

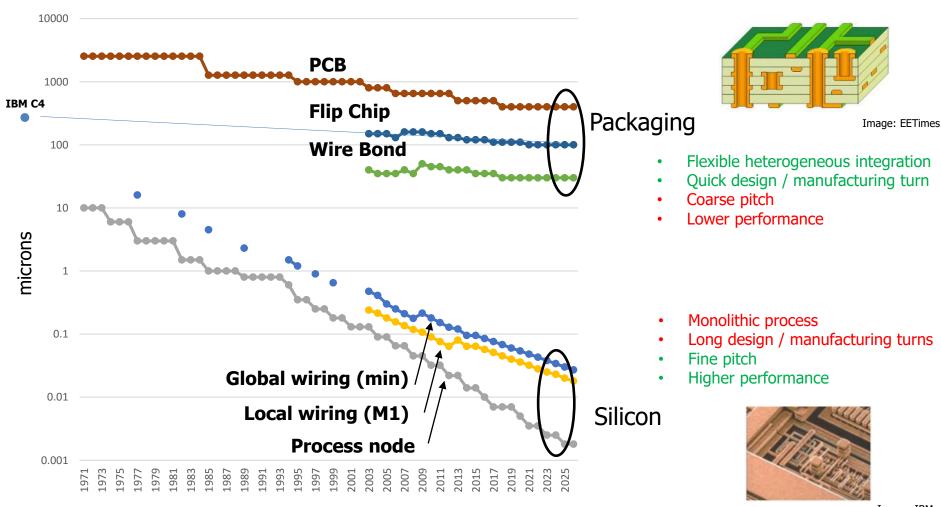
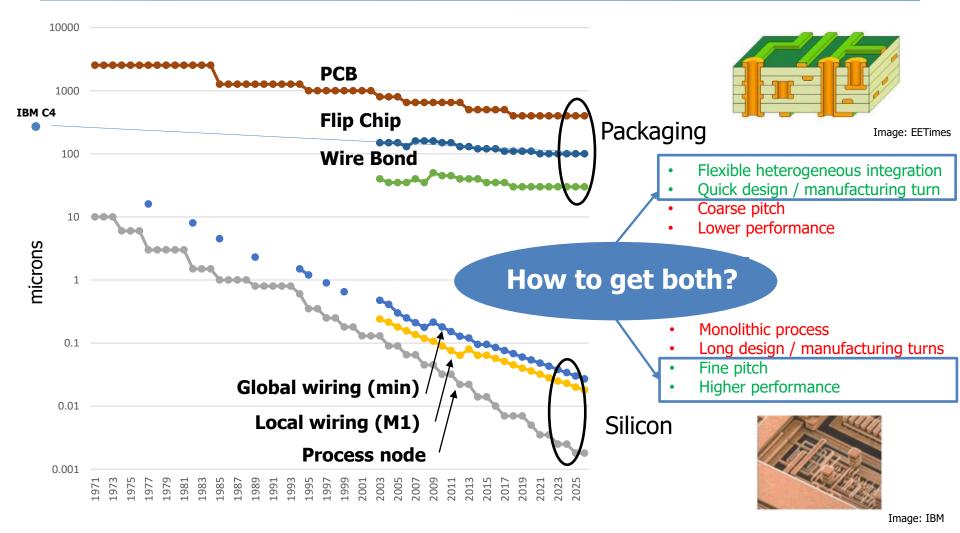


Image: IBM

Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.



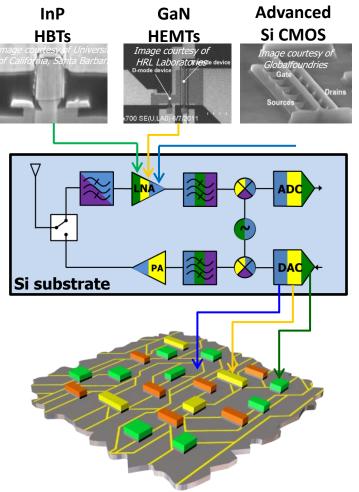
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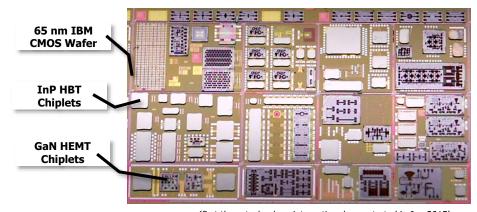
Need to combine speed and flexibility of packaging with pitch and performance of advanced heterogeneous device technology.



Diverse Accessible Heterogeneous Integration (DAHI) Foundry for Heterogeneous Integration



Heterogeneous technology integration in accessible foundry



(first three-technology integration demonstrated in Jan 2015)

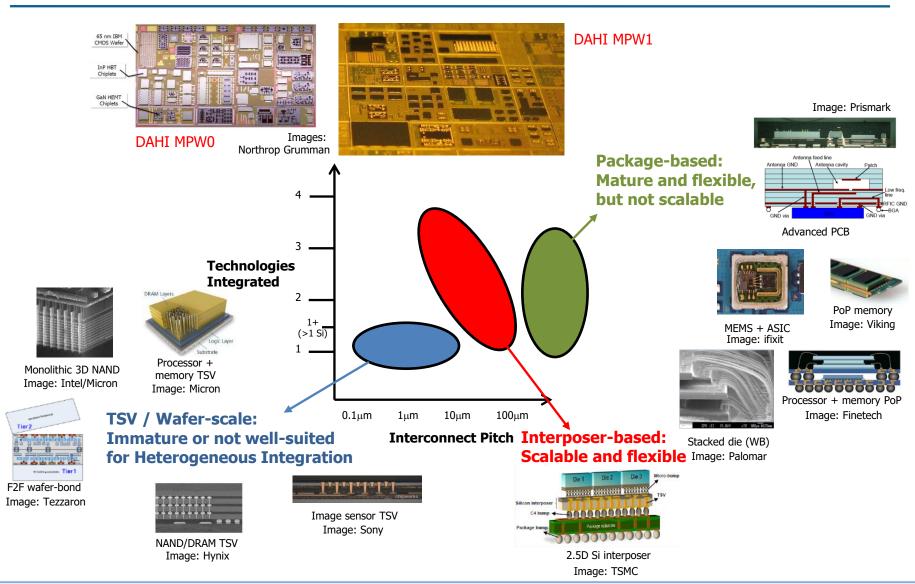
Image: Northrop Grumman

Heterogeneous Integration of a diverse array of devices on a common Si CMOS platform

Goal: To establish a versatile platform of heterogeneous integration that enables pervasive impact on DoD systems.



DARPA Heterogeneous Integration: Bridging the Gap



DAHI creates integration capabilities beyond current advanced interconnect technologies.

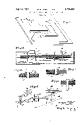


Propelled by **Standards** and **Modularity**: Electronics Industry Built via Integration on PCBs







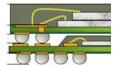












"Printed circuit board" invented by Paul Eisler.

Early PCB demo in a radio.

First HVM PCBs enable proximity fuze during WWII.

Patent to **US Army** for PCB assembly.

IPC (Institute for Printed Circuits) founded: standards follow.

Image: Intel Multilayer PCB invented.

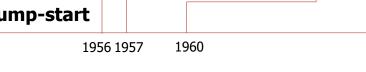
Surface Mount Technology on PCBs revolutionizes manufacturing.

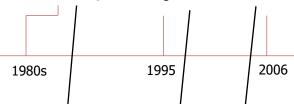
HDI / Microvia technology enables further integration.

First packageon-package standard from JEDEC.

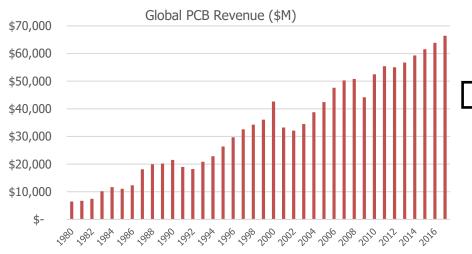


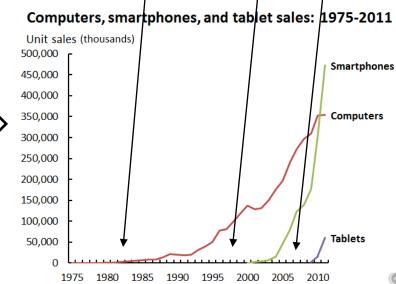


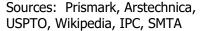




PCB industry sees steady expansion with DoD origins, standardization, and technology development.

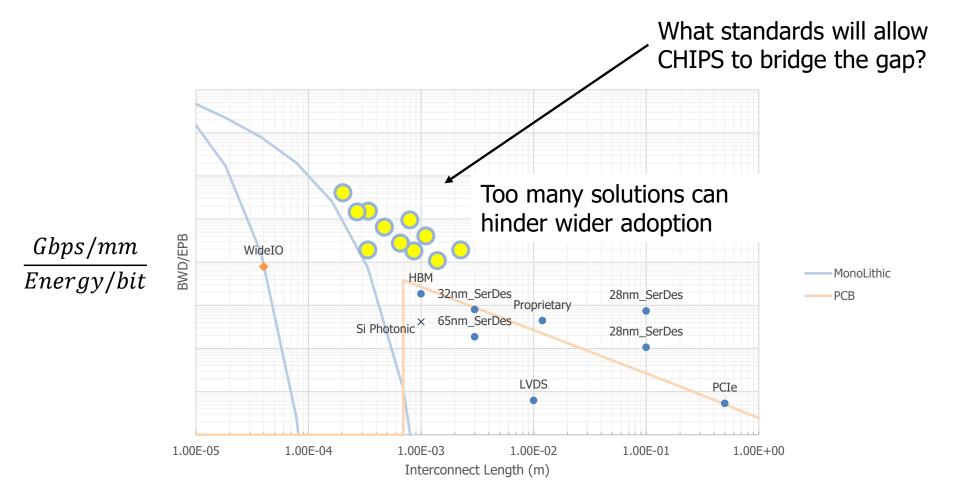








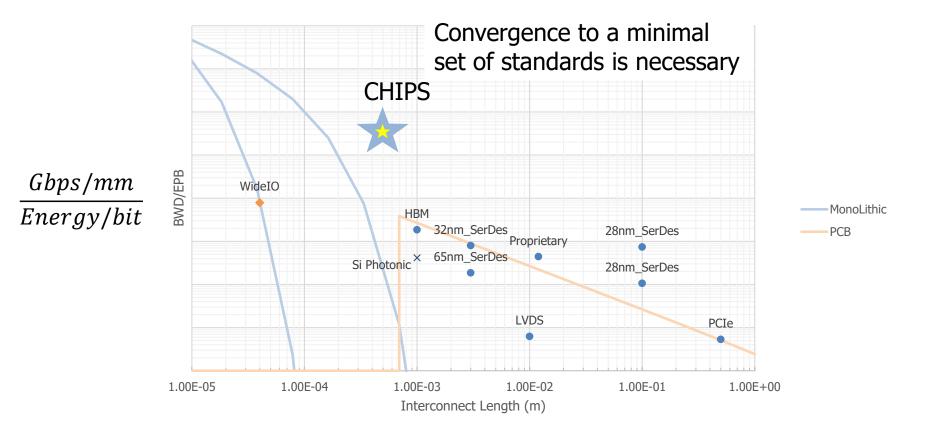
Interface Standards: Too Many? Not Enough? How to Compare?



CHIPS challenge: make a usable interface standard



Interface Standards: Too Many? Not Enough? How to Compare?



CHIPS challenge: make a usable interface standard

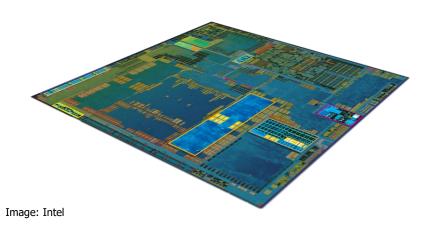


So what do we plan to do?

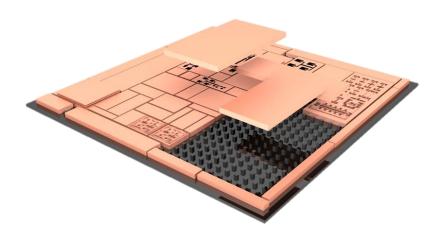


CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic



Tomorrow – Modular



CHIPS is focused on creating modular IP – not new IP!



DARPA CHIPS Program – Structure and Timing

PHASE 1	PHASE 2	PHASE 3	
Interface and IP Block Demo	Module Demo with IP Blocks	Rapid Module Upgrade	
Integration platform Interface demo	Full system IP reuse demo	Reconfigured demo	
Phase 1a (8 mo.) M1 – Interface standards CDR Phase 1b (10 mo.) M1 – Interface M3 – Module PD	Phase 2 (18 mo.) demo M4 – Module de		
	TA1 Modular Digi TA3 Supporting T	, , , , , , , , , , , , , , , , , , ,	
•	TA2 Modular Ana	log Systems	



DARPA CHIPS Program - Metrics

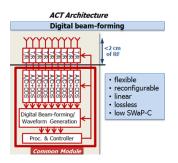
CHIPS Program Metrics				
Metric	Phase 1	Phase 2	Phase 3	
Design level				
IP reuse (1)	> 50% public IP blocks	> 50% public IP blocks	> 50% public IP blocks	
Modular design (2)	_		> 80% reused, > 50% prefabricated IP	
Access to IP (3)	> 2 sources of IP	> 2 sources of IP	> 3 sources of IP	
Heterogeneous integration (4)	> 2 technologies	> 2 technologies	> 3 technologies	
NRE reduction (5)	_	> 50%	>70%	
Turnaround time reduction (5)	_	> 50%	>70%	
Performance Benchmarks (performer defined)	_	>95% benchmark	>100% benchmark	
Digital Interfaces				
Data rate (scalable) (6)	10 Gbps	10 Gbps	10 Gbps	
Energy efficiency (7)	< 1 pJ/bit	< 1 pJ/bit	< 1 pJ/bit	
Latency (7)	≤ 5 nsec	≤ 5 nsec	≤ 5 nsec	
Bandwidth density	> 1000 Gbps/mm	> 1000 Gbps/mm	> 1000 Gbps/mm	
Analog interfaces				
Insertion loss (across full bandwidth)	< 1 dB	< 1 dB	< 1 dB	
Bandwidth	≥ 50 GHz	≥ 50 GHz	≥ 50 GHz	
Power Handling	≥ 20 dBm	≥ 20 dBm	≥ 20 dBm	

Notes:

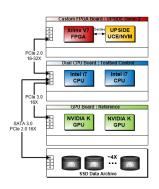
- 1. Public IP is defined as IP blocks available through commercial vendors or shared among performers.
- 2. Reuse is defined as existing or previously designed IP that is re-implemented into the current system. Prefabricated IP is defined as IP blocks already physically instantiated.
- 3. Valid sources of IP must be those that are outside of the performer team.
- 4. Various Silicon process nodes, RF passives, or compound semiconductor devices.
- 5. The non-recurring engineering (NRE) cost and turnaround time will be compared against a benchmark design.
- 6. Minimum bus/lane data rate and should be capable of scaling to higher data rates.
- 7. Performance relating to transferring data between chiplets compared against a benchmark design.



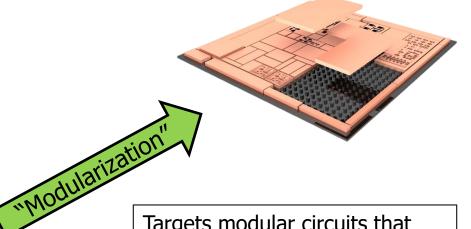
DARPA TA1: Modular Digital Systems



Arrays at Commercial Timescales (ACT)



Unconventional Processing of Signals for Intelligent Data Exploitation (UPSIDE)



Targets modular circuits that leverage digital interfaces.

Looking for designs that:

- Leverage modular interface
- · Reuse existing IP
- Are DoD relevant

Includes:

- Analog/Mixed signal circuits with digital interface
- non-DARPA designs



Cortical Processor



Semiconductor Technology Advanced Research Network (STARnet)

Others: CLASS, Mobile Hotspots, MFRF, ViSAR, ELASTx, ...

Don't need to start from scratch!



DARPA TA2: Modular Analog Systems

RF Unit Cell

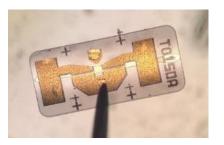
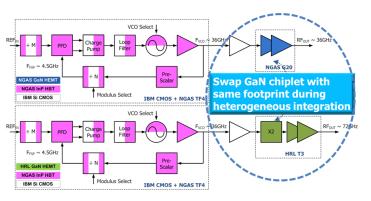
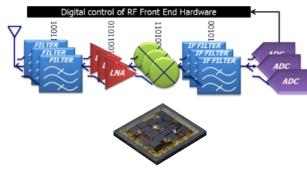


Image: NRL

Modular Devices



Modular Signal Blocks



Range of analog building block granularity

Seeks to realize modular pseudolithic microwave integrated circuits:

- Leverage modular building blocks
- Demonstrate performance into mm-Wave regime
- Develop sustainable attractive business models

Balance granularity with accessibility, reusability and cycle time



DARPA TA3: CHIPS Supporting Technologies

- Design tools
 - Heterogeneous integration
 - Modular design flows
- Assembly methods

Design Tools

Design

- Fine pitch
- Small device handling / testing

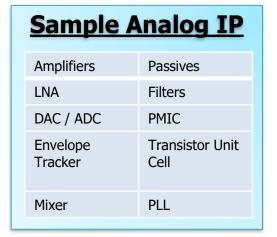
Layout

- Multi-device technology processing
- IP blocks

Simulation

Assembly	Methods
23 7 A 22 A 22 A 22 A 23 A 24 A 24 A 24 A 24	
Fine pitch interconnects	Heterogeneous integration
interconnects	integration
Images: Northrop Grumman	

Sample Digital IP		
Processor	Interface	Memory
Image signal	SerDes	Controller
Audio signal	USB	DRAM
Digital signal	PCIe	SRAM
Compression		Flash
GPU		
CPU		
Machine Learning		



Key challenge will be alignment to TA1 and TA2



DARPA Non-CHIPS Developments

Technology NOT germane to CHIPS:

- New device technologies
- Wholly new circuits
- Security specific processes (e.g. obscuration, split fabrication)

Focus is on making modularity work!



CHIPS end state vs. conventional supply chain

	IP Blocks	CAD tools	Architecture	Design	Verification	Fabrication	Pkg / Test	Systems
Commercial	ARM TSMC Cadence Imagination	Cadence Mentor Graphics Synopsys	Google Apple Microsoft Samsung	Qualcomm Broadcom Apple TI Marvell	Qualcomm Broadcom Apple TI Marvell	TSMC SMIC GlobalFoun. Intel Samsung	TSMC ASE Group Amkor	Google Apple Microsoft Samsung
DoD	ARM Global Foundries	Cadence Mentor Graphics Synopsys	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE	Northrop TowerJazz HRL Global Foundries	Raytheon Northrop Lockheed Boeing BAE	Raytheon Northrop Lockheed Boeing BAE
CHIPS	ARM TSMC Cadence Imagination Raytheon Northrop Lockheed Boeing	Cadence Mentor Graphics Synopsys	Raytheon Northrop Lockheed Boeing BAE		CHIPS		Northrop Novati US OSAT	Raytheon Northrop Lockheed Boeing BAE
	BAE		Design specs	Chiplet	s	•		
à	Note: Compani re examples o	nly.)		\Longrightarrow	TSMC Intel Global Foundries	Northrop Raytheon HRL	Jariet ? Intrinsix Flexlogix	Mouser Digi-Key
_	Trusted sou	rces for cr	itical compo	onents	Commercial	Defense	Emerging	Distributor



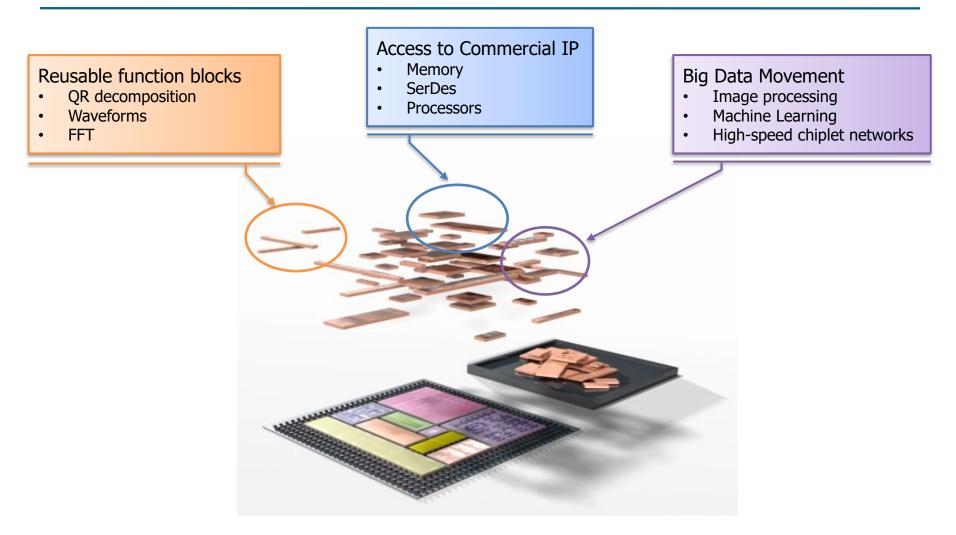
DARPA CHIPS Program – Program Summary

PHASE 1	PHASE 2	PHASE 3
Interface and IP Block Demo	Module Demo with IP Blocks	Rapid Module Upgrade
Integration platform Interface demo	Full system IP reuse demo	Reconfigured demo

	TA1 Modular Digital System	IS
 Modularize existing digital design via interface standard. Critical design review for standards at 8-month mark. Demonstrate functional IP blocks. 	 Demonstrate functional digital design. Cost + design cycle analysis. Present design for Phase3. 	 Demonstrate rapid upgradability. Cost + design cycle analysis comparing CHIPS module versus a monolithic implementation.
	TA2 Modular Analog System	is
 Modularize existing analog design via interface standard. Review design and interface at the 8-month mark. Demonstrate interconnect performance. 	 Integrate blocks into PLIC. Analyze against SoA for performance, unit cost, NRE, and turnaround time. Develop business model for modular analog ecosystem. 	 Demonstrate rapid assembly of new PLICs. Analyze against SoA for performance unit cost, NRE, and turnaround time. Cost / development time analysis of CHIPS PLIC vs MMIC.
	TA3 Supporting Technologie	es es



DARPA What CHIPS Means for the DOD



CHIPS modularity targets the enabling of a wide range of custom solutions



What do we plan to spend? and When?

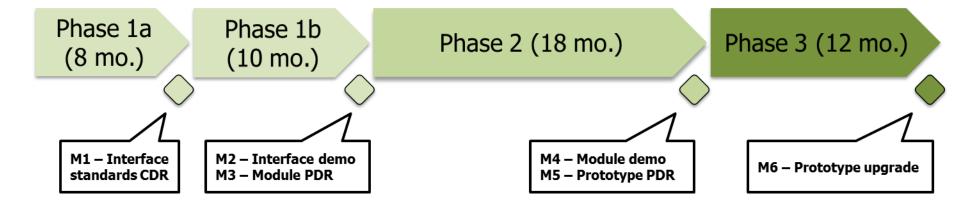
- Anticipated Funding Available for Award: DARPA anticipates a funding level of approximately \$70M for the CHIPS program.
- Anticipated individual awards Multiple awards in each Technical Area are anticipated.
- Anticipated funding type 6.2 and/or 6.3
- Types of instruments that may be awarded Procurement contract, grant, cooperative agreement or other transaction.

Important Dates		
Proposers Day	21-Sep-2016	
BAA Release (est.)	26-Sep-2016	
Abstracts Due*	26-Oct-2016	
FAQ Deadline*	23-Nov-2016	
Proposals Due*	7-Dec-2016	
Program Kick-Off*	Mar-2017	

^{*}Dates are a function of actual BAA release date.







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TA1	Modular Digital Systems
TA2	Modular Analog Systems
TA3	Supporting Technologies

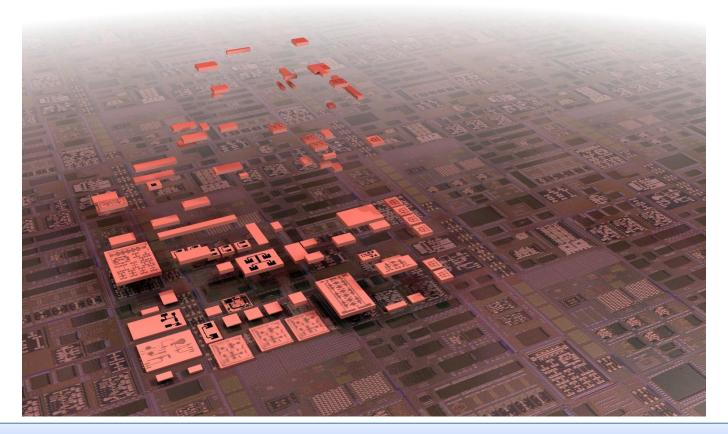
Questions: DARPA-BAA-16-62@darpa.mil

^{*}Dates are a function of actual BAA release date.



DARPA CHIPS future of heterogeneous integration





Requires a lot of pieces coming together!



